CA-IS37XX Single/Dual Channels Digital Isolator Evaluation Module

This user's guide describes the CA-IS37xx single/dual channels Digital Isolator Evaluation Module (EVM). This EVM allows designers to evaluate device performance for fast development and analysis of isolated systems. The EVM supports evaluation of any of the CA single/dual channel digital isolators in a SOP8 package.

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1. Introduction

This user's guide describes EVM operation with respect to the CA-IS37xx dual-channel digital isolators. However, the EVM may be reconfigured for evaluation of any of CA's dual-channel digital isolators in a SOP8 package. This guide also describes the available channel configurations within the CA-IS37xx family, the EVM schematic, and typical laboratory setup. A typical input and output waveform is also presented.

2. Overview

The CA-iS37xx is CA's new digital isolator family. The devices are certified to meet reinforced isolation requirements by VDE and CSA. These isolators provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/O's. The CA-IS37xx digital isolators have logic input and output buffers separated by a silicon oxide (SiO2) insulation barrier. Used with isolated power supplies, these devices block high voltages, isolate grounds, and prevent noise currents on a data bus or other circuits from entering the local ground and interfering with, or damaging sensitive circuitry.

3. Pin Configurations of the CA-IS37xx Single/Dual-Channel Digital Isolators

Figure 1 illustrates the CA-IS37xx dual-channel digital isolator pin configurations.

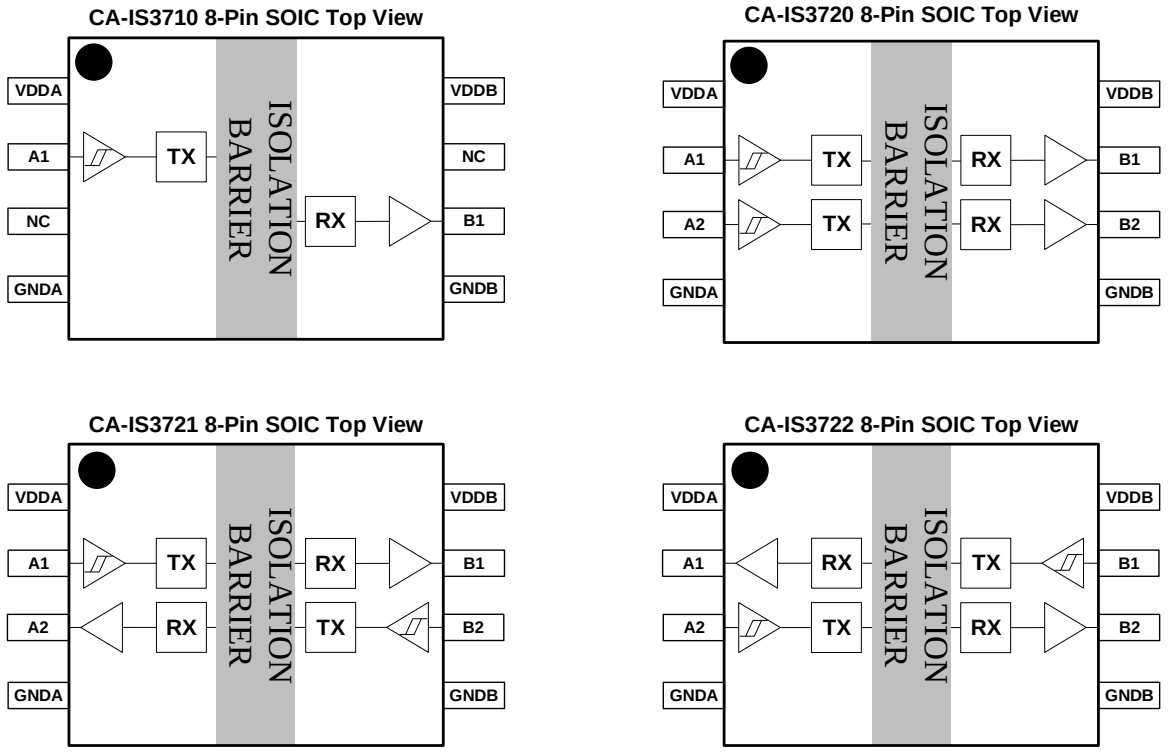

Figure 1 the CA-IS37xx single/dual-channel digital isolator pin configurations

4. CA-IS3722 – EVM Board Block Diagram and Image

Figure 3 shows the board configuration for evaluation of the CA-IS3722 dual-channel digital isolator.

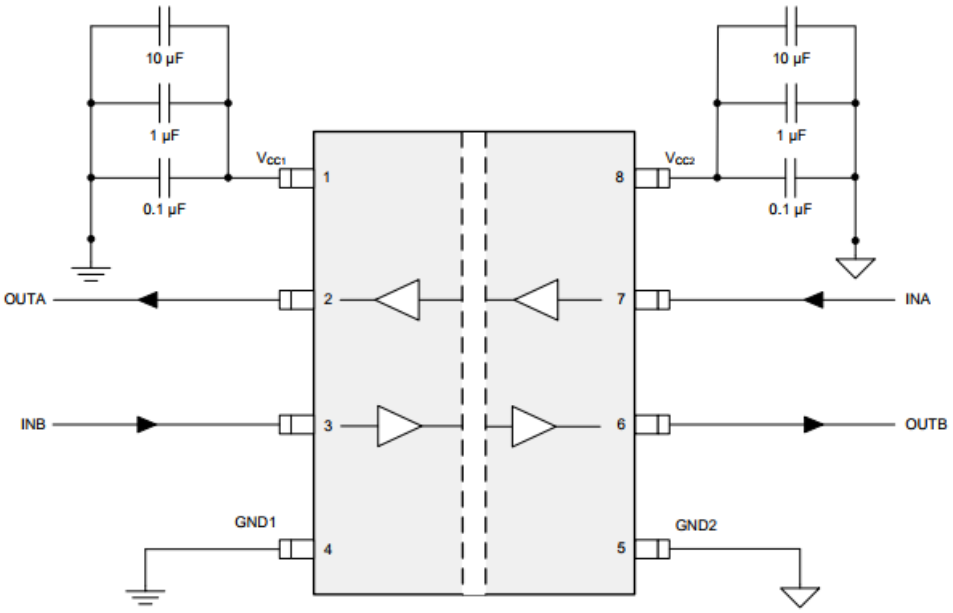

Figure 2 CA-IS3722 EVM Configuration

Figure 4 shows the photograph of the EVM.

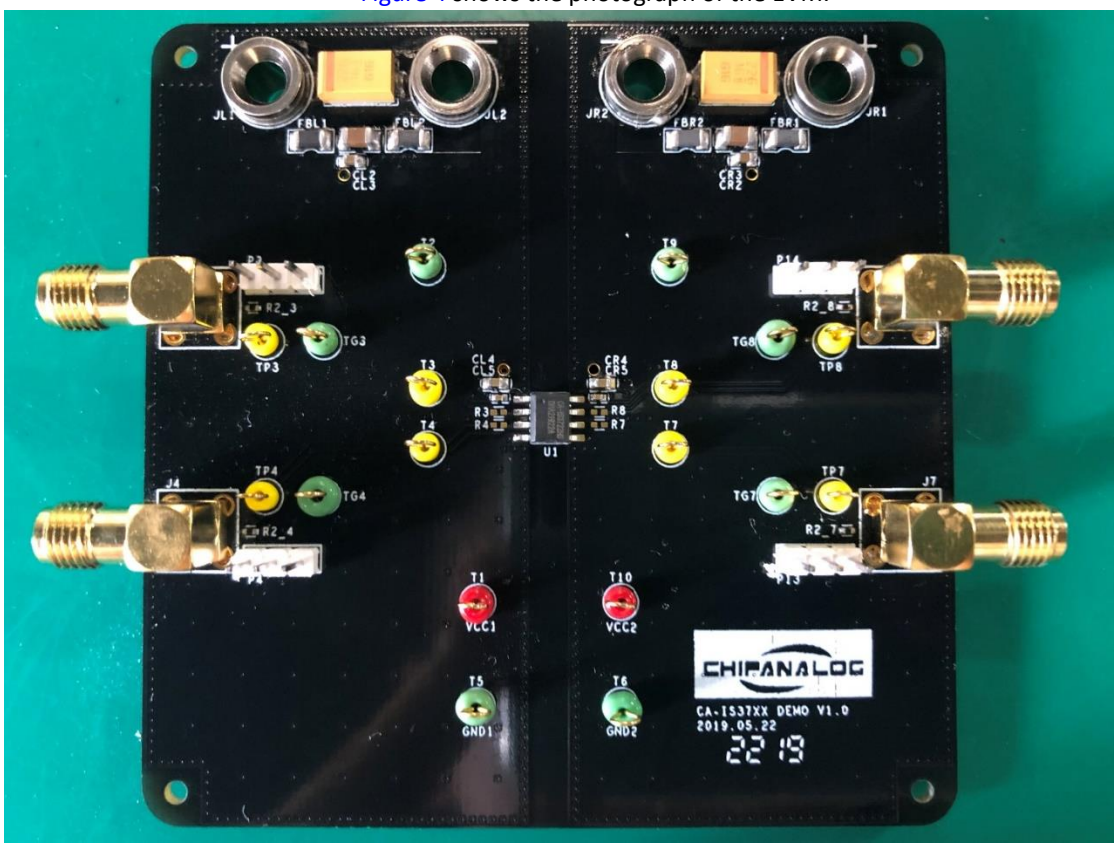

Figure 3 CA-IS37xx-EVM photograph

5. EVM Setup and Operation

This section describes the setup and operation of the EVM for parameter performance evaluation. Figure 5 shows the configuration for operating the CA-IS37XX Triple/Quad Digital Isolator EVM using two power supplies.

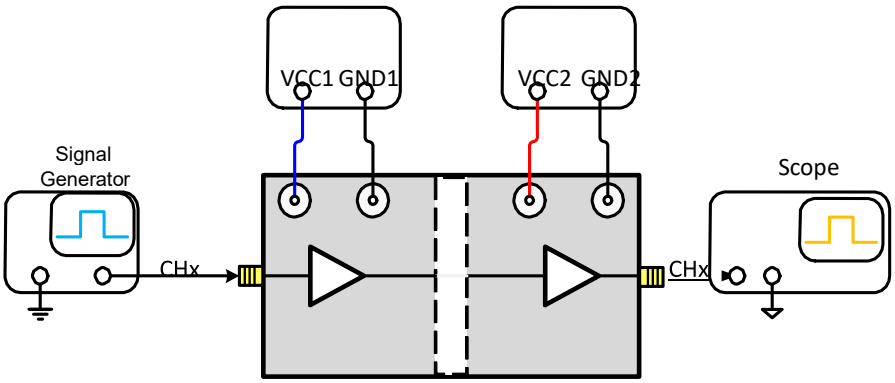

Figure 4 the basic EVM operation

Figure 6 shows typical input and output waveforms of the EVM for a 0.5MHz clock. The input is shown as channel 1, and the output is shown as channel 2.

Figure 5 typical input and output waveforms

6. Bill of Materials

Table 1 bill of materials

Item	Quantity	References	Value	Footprint
1	2	CL1,CR1	22uF	7343
2	2	CL2,CR2	10uF	1206
3	4	CL3,CL4,CR3,CR4	1uF	0603
4	2	CL5,CR5	0.1uF	0402
5	4	FBL1,FBL2,FBR1,FBR2	600 Ω	1206
7	4	JL1,JL2,JR1,JR2	BANANA	BANANA
8	10	J3,J4,J7,J8	SMA	SMA
9	10	P3,P4,P13,P14	3 pin Header	Header
10	10	R2_3,R2_4,R2_7,R2_8	10K Ω	0402
12	2	T1,T10	Test Point	Test Point
13	14	T2,T5,T6,T9,TG3,TG4,TG7,TG8	Test Point	Test Point
14	20	T3,T4,T7,T8,TP3,TP4,TP7,TP8	Test Point	Test Point

7. EVM Schematics and Layout

Separate orderable EVMs are available for each triple- and quad-channel device in the CA-IS37xx family of digital isolators. The EVMs need to be modified only in the placement of 50-Ω termination resistors at the input, and 10-pF capacitive loads at the output (if needed) of each channel. Figure 6 shows the CA-IS37xx EVM schematic and Figure 7 shows the printed-circuit board (PCB) layout.

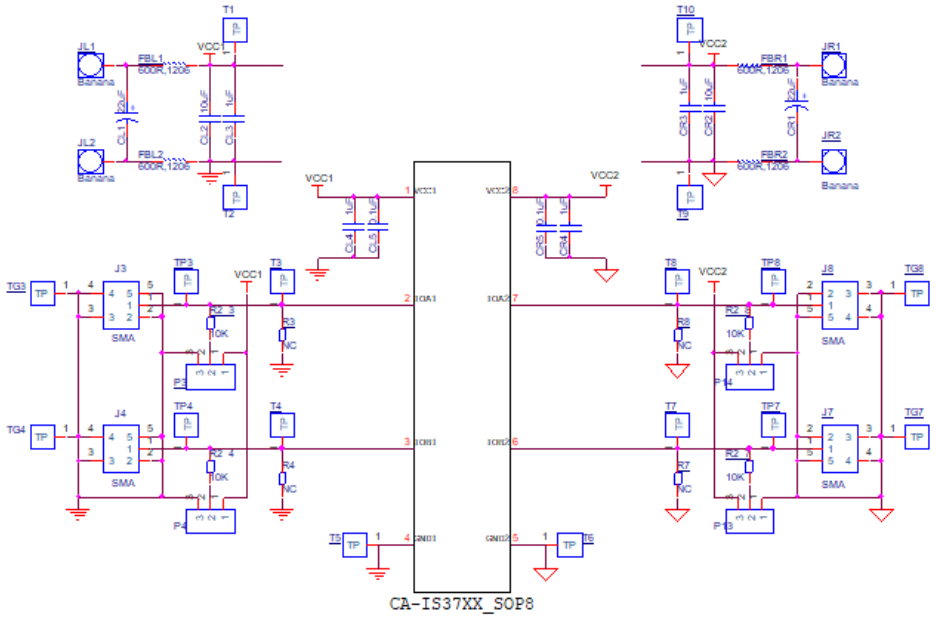

Figure 6 CA-IS37XX_SOP8 (N/W) EVM Schematic

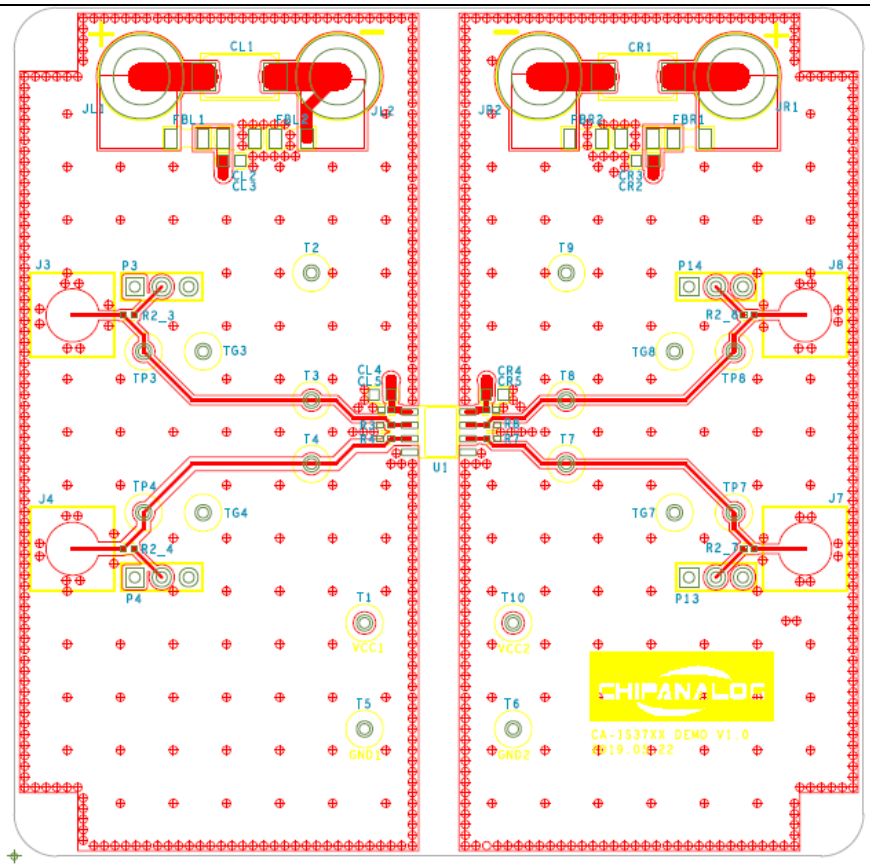

Figure 7 CA-IS37XX_SOP8 PCB layout