CA-IS37XX Triple/Quad Digital Isolator Evaluation Module

This user's guide describes the CA-IS37xx Triple/Quad Digital Isolator Evaluation Module (EVM). This EVM allows designers to evaluate device performance for fast development and analysis of isolated systems. The EVM supports evaluation of any of the CA triple- or quad-channel digital isolators in a SOP16 package.

Contest

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1.   Introduction

This user's guide describes EVM operation with respect to the CA-IS37xx triple- and quad-channel digital isolators. However, the EVM may be reconfigured for evaluation of any of CA's triple- or quad-channel digital isolators in a SOP16 package. This guide also describes the available channel configurations within the CA-IS37xx family, the EVM schematic, and typical laboratory setup. A typical input and output waveform is also presented.

2.   Overview

The CA-iS37xx is CA's new digital isolator family. The devices are certified to meet reinforced isolation requirements by VDE and CSA. These isolators provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/O's. The CA-IS37xx digital isolators have logic input and output buffers separated by a silicon oxide (SiO2) insulation barrier. Used with isolated power supplies, these devices block high voltages, isolate grounds, and prevent noise currents on a data bus or other circuits from entering the local ground and interfering with, or damaging sensitive circuitry.

3.   Pin Configurations of the CA-IS37xx Triple- and Quad-Channel Digital Isolators

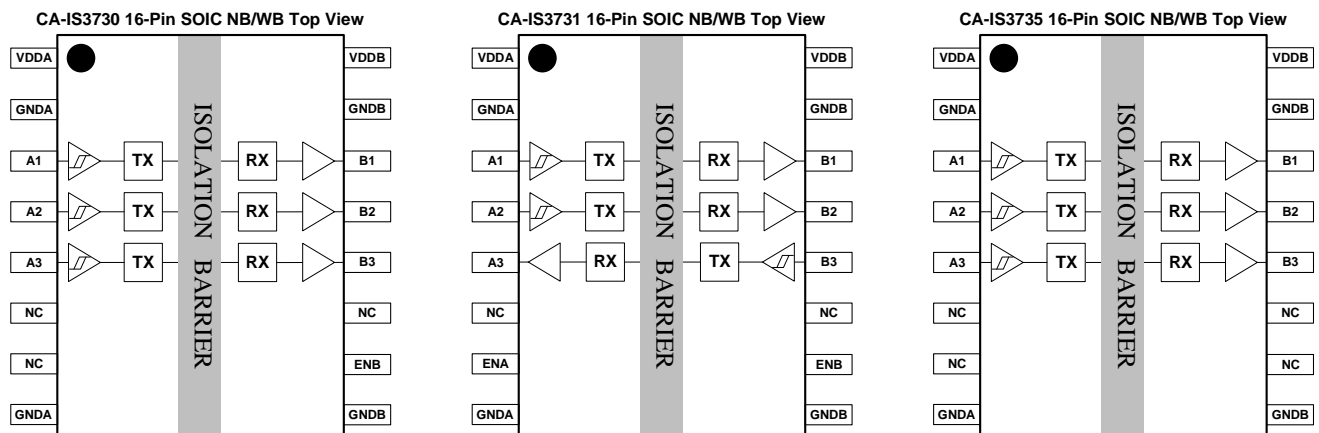Figure 1 illustrates the CA-IS37xx triple-channel digital isolator pin configurations.

Figure 1 the CA-IS37xx triple-channel digital isolator pin configurations

Figure 2 illustrates the CA-IS37xx quad-channel digital isolator pin configurations.
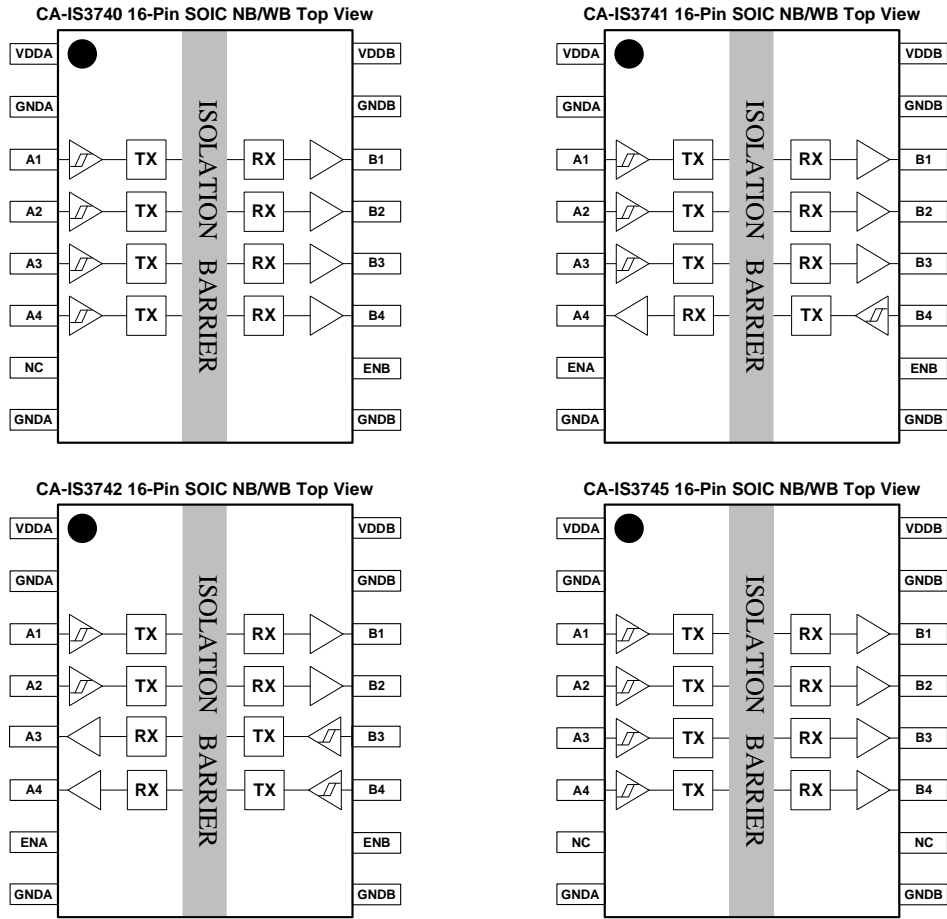
CA-IS3740 16-Pin SOIC NB/WB Top View

CA-IS3741 16-Pin SOIC NB/WB Top View

CA-IS3742 16-Pin SOIC NB/WB Top View

CA-IS3745 16-Pin SOIC NB/WB Top View

Figure 2 the CA-IS37xx quad-channel digital isolator pin configurations

4. CA-IS3742 – EVM Board Block Diagram and Image

Figure 3 shows the board configuration for evaluation of the CA-IS3742 quad-channel digital isolator.
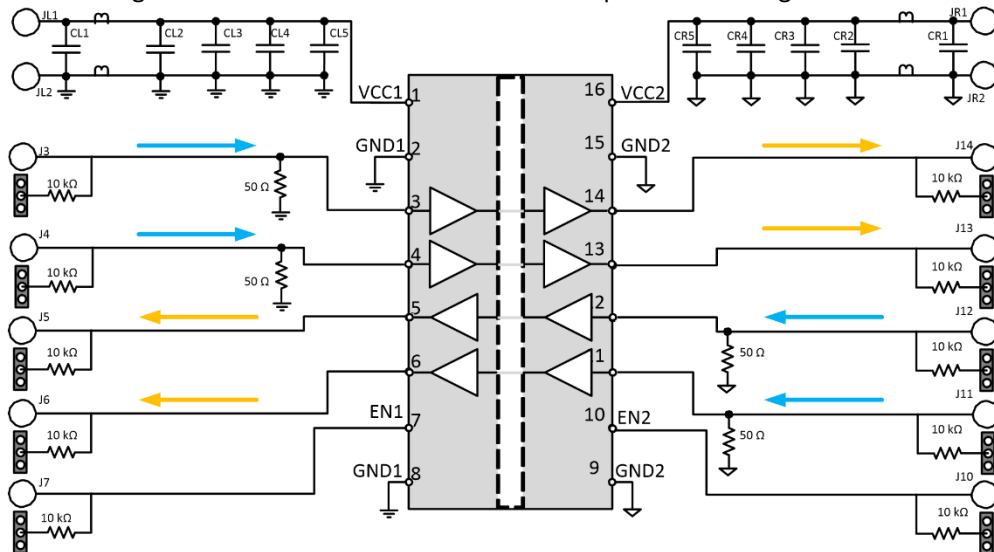
Figure 3 CA-IS3742 EVM Configuration
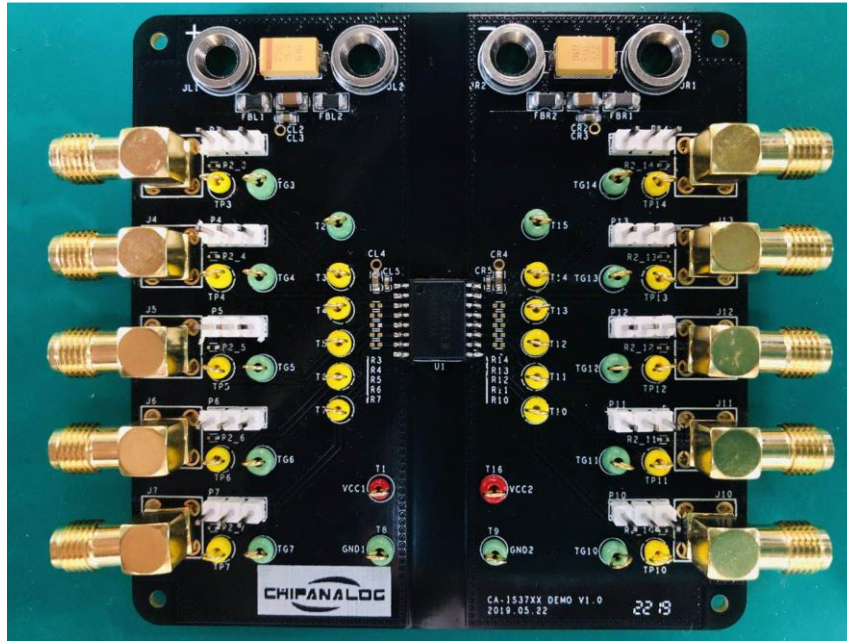
Figure 4 shows the photograph of the EVM.

Figure 4 CA-IS37xx-EVM photogragh

5. EVM Setup and Operation

This section describes the setup and operation of the EVM for parameter performance evaluation. Figure 5 shows the configuration for operating the CA-IS37XX Triple/Quad Digital Isolator EVM using two power supplies.
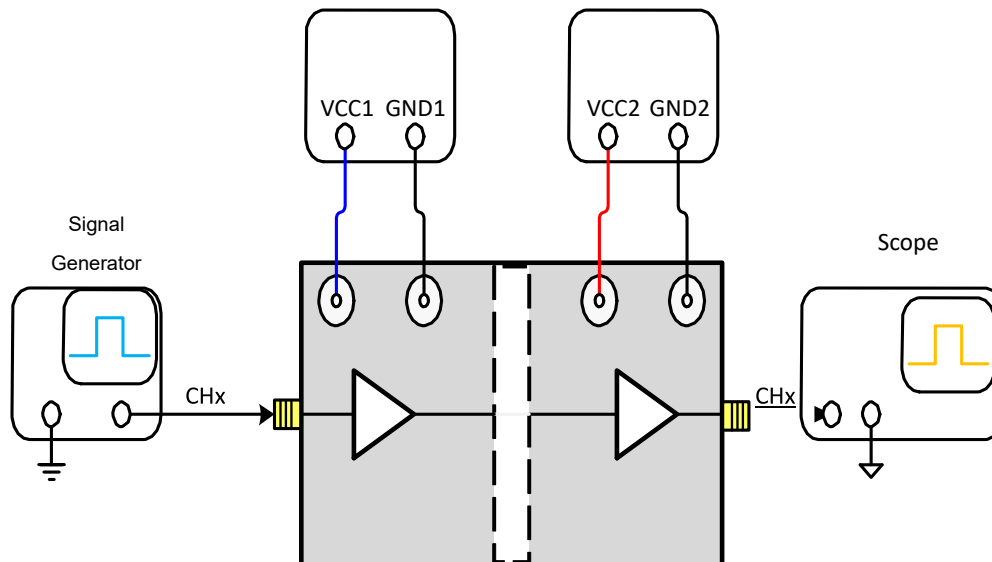

Figure 5 the basic EVM operation

Figure 6 shows typical input and output waveforms of the EVM for a 0.5MHz clock. The input is shown as channel 1, and the output is shown as channel 2.
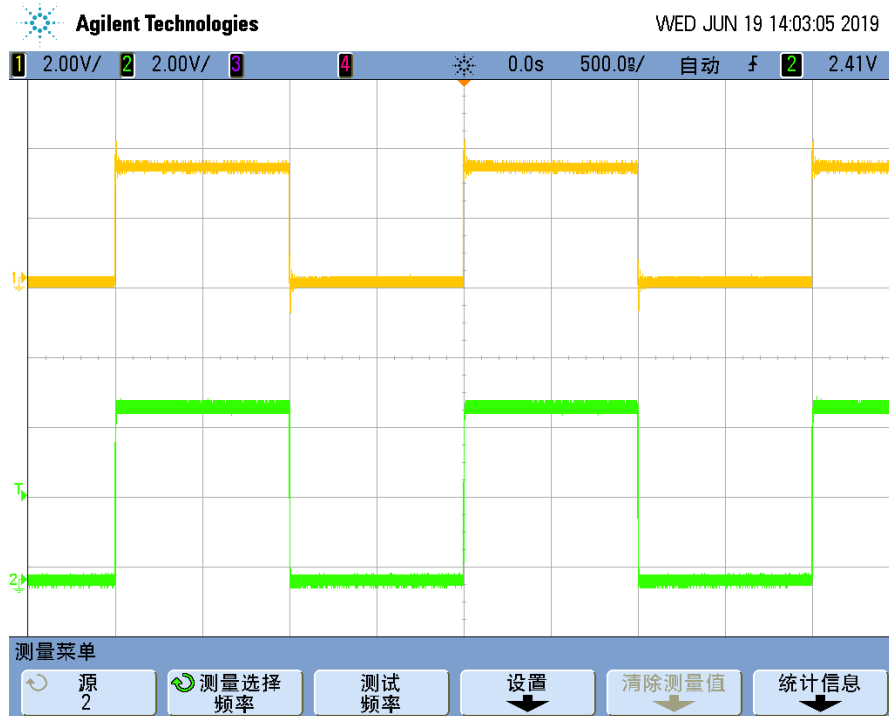

Figure 6 typical input and output waveforms

6.   Bill of Materials

Table 1 bill of materials

Item	Quantity	References	Value	Footprint
1	2	CL1,CR1	22uF	7343
2	2	CL2,CR2	10uF	1206
3	4	CL3,CL4,CR3,CR4	1uF	0603
4	2	CL5,CR5	0.1uF	0402
5	4	FBL1,FBL2,FBR1,FBR2	600 Ω	1206
7	4	JL1,JL2,JR1,JR2	BANANA	BANANA
8	10	J3,J4,J5,J6,J7,J10,J11,J12,J13,J14	SMA	SMA
9	10	P3,P4,P5,P6,P7,P10,P11,P12,P13,P14	3 pin Header	Header
10	10	R2_3,R2_4,R2_5,R2_6,R2_7,R2_10,R2_11,R2_12,R2_13,R2_14	10K Ω	0402
12	2	T1,T16	Test Point	Test Point
13	14	T2,T8,T9,T15,TG3,TG4,TG5,TG6,TG7,TG10,TG11,TG12,TG13,TG14	Test Point	Test Point
14	20	T3,T4,T5,T6,T7,T10,T11,T12,T13,T14,TP3,TP4,TP5,TP6,TP7,TP10, TP11,TP12,TP13,TP14	Test Point	Test Point

7.   EVM Schematics and Layout

Separate orderable EVMs are available for each triple- and quad-channel device in the CA-IS37xx family of digital isolators. The EVMs need to be modified only in the placement of 50-Ω termination resistors at the input, and 10-pF capacitive loads at the output (if needed) of each channel. Figure 7 shows the CA-IS37xx EVM schematic and Figure 8 shows the printed-circuit board (PCB) layout.
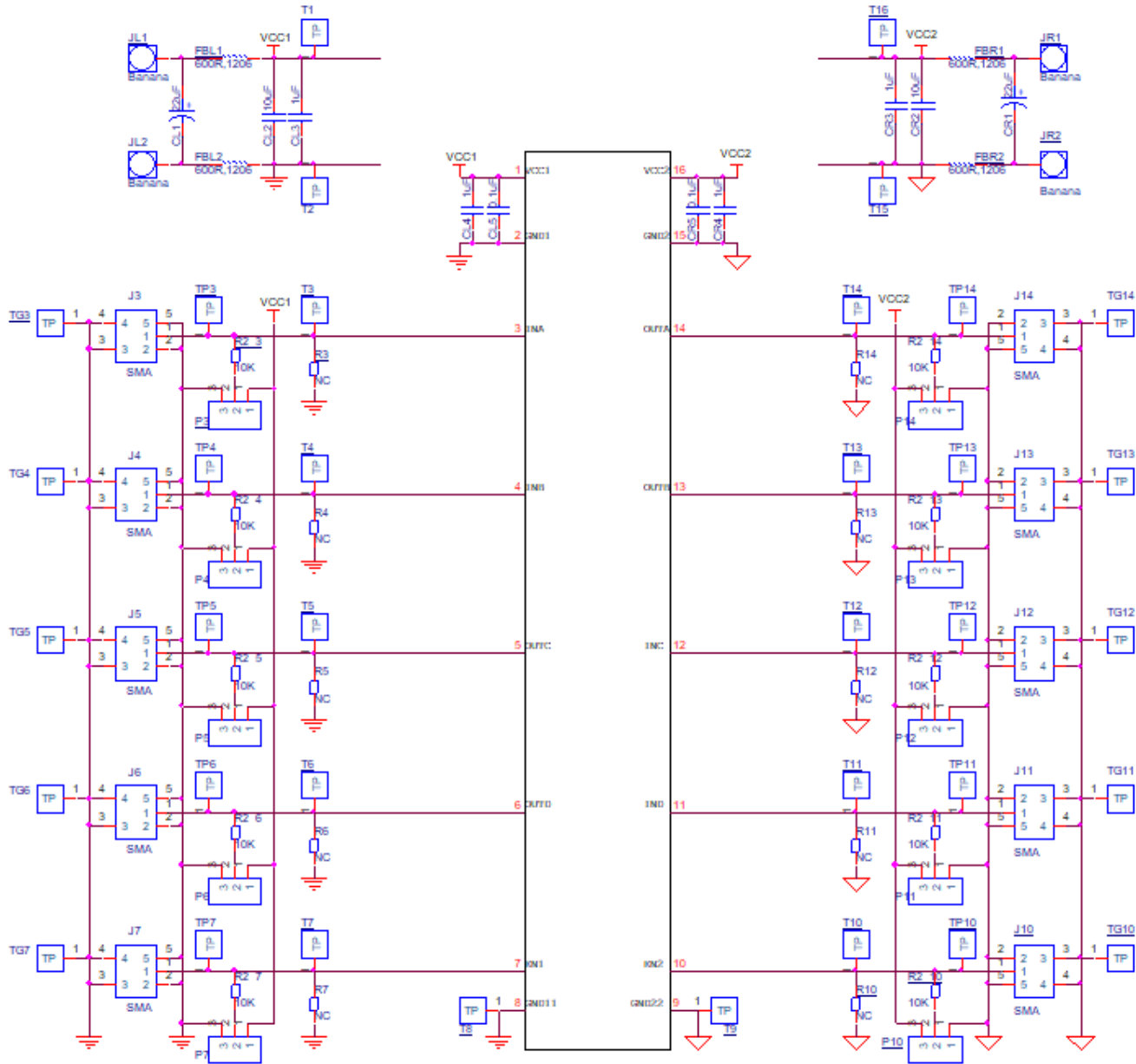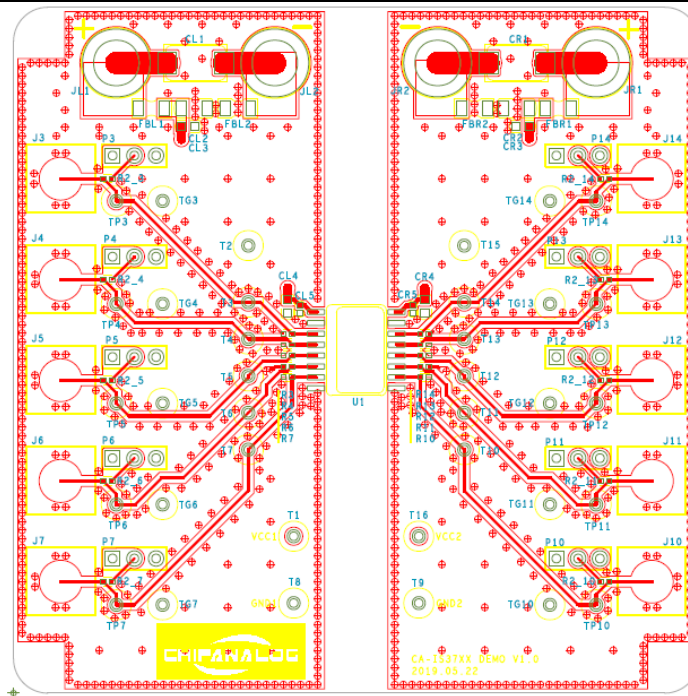

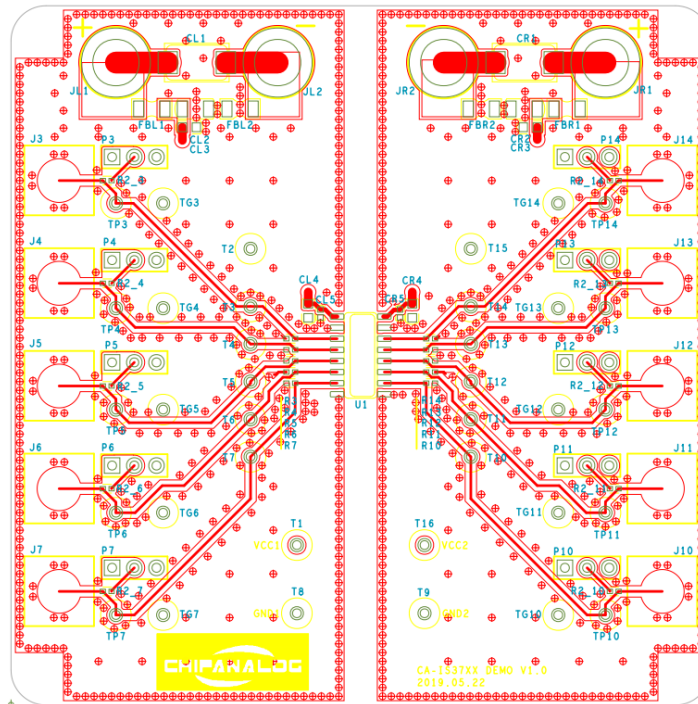**Figure 7 CA-IS37XX_SOP16 EVM schematic**

Figure 8 CA-IS37XX_SOP16W EVM PCB layout

Figure 9 CA-IS37XX_SOP16N EVM PCB layout